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Application Note 092

Data Acquisition Specifications – a Glossary

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Introduction

This application note consists of comprehensive descriptions of the specifications that National Instruments uses to characterize the performance of its data acquisition (DAQ) products. It is intended to make it easier to interpret and understand the material in our Instrumentation Reference and Catalogue.

Specifications

Note: ***All specifications represent typical performance at 25°C unless otherwise noted. Not all specifications are applicable for all DAQ products.***

Analog Input

Input Characteristics

Number of Channels – The number of analog signals that the DAQ product is able to digitize. Usually, this specification groups the channels into single-ended, pseudodifferential, and differential channels. Single-ended channels have all inputs referred to a common ground that is connected to the computer ground. Pseudodifferential channels are all referred to a common ground but this ground is not connected to the computer ground. Differential inputs have an independent reference for each channel, none of which is connected to the computer ground. For more information on which type of input is best for your application, see National Instruments Application Note 025, *Field Wiring and Noise Considerations for Analog Signals.*

Type of ADC – Different applications require different types of analog-to-digital converters (ADCs) for optimal performance. For example, an AC-class signal will most often be measured best with a delta-sigma modulating ADC. Common types of ADCs include successive approximation, flash, half-flash, integrating, and delta-sigma modulating.

Resolution – The number of bits that the ADC uses to represent the analog signal. The higher the resolution, the greater the number of divisions the range is broken into, and therefore, the smaller the detectable voltage change for a given input range and gain. The smallest detectable voltage change for an ideal DAQ board is determined by:

$$\text{Smallest detectable voltage change} = \text{range}/(\text{gain}*2^{\text{resolution}})$$

Resolution is only one indication of the accuracy of a DAQ product. You must consider at least the relative accuracy (linearity), settling time, offset errors, and gain errors to fully understand the accuracy of a DAQ product.

Max Sampling Rate – The highest rate at which the input circuitry can digitize the analog signal. The product will most likely have many other slower rates at which the product can digitize. For multichannel sampling, the maximum sampling rate may not be achievable with full accuracy unless the instrumentation amplifier settles properly as defined by the settling time specification. For a complete description of settling time, see National Instruments Application Note 045, *Is Your Data Inaccurate Because of Instrumentation Amplifier Settling Time?*

Input Signal Ranges – The voltage ranges that the DAQ product can be configured to accept and convert accurately. National Instruments combines the input range and gain in one table to concisely specify the input range, gain, and actual input signal range. You can calculate the actual input signal range for products that do not specify it by:

actual input signal range = input range/gain

For example, an input range of 0 to 10 V with a gain of 100 means that the product can accept signals from 0 to 0.1 V. Input range and gain are selected in hardware on some products and by software on others. The Maximum Working Voltage specification is related to the input signal range for signals with a common-mode voltage and the Overvoltage Protection specification indicates how far you can exceed the input signal range without damaging the product.

Input Coupling – The method by which the input signals are connected to the analog input circuitry. If the coupling is DC, both AC and DC portions of signals are passed. If the coupling is AC, then only AC portions of signals are passed and any DC portions are rejected.

Maximum Working Voltage (signal + common mode) – The highest voltage level that can be input to the board without saturating the input. Even though a signal input range may be as small as 0 to 0.1 V, both signals of a differential pair may be added to a common-mode voltage that is outside the range of the board and therefore saturate the inputs. Sometimes, this specification is simply called the common-mode voltage even though it refers to a combination of the common-mode voltage and the signal voltage.

Overvoltage Protection – The highest voltage level that can be input to the board without damaging the board. Usually, a specification will be given for when the board is powered on and when the board is powered off. It is important to note that for a differential pair, a low voltage signal that is added to a high common-mode voltage can damage the board if the combination of the differential and common mode voltages exceed the level to which the board is protected.

Channels Protected – The names of the channels that have overvoltage protection.

Input Damage Level – The highest voltage level that can be input to the module without damaging the module. The application of voltages up to this level, however, is not necessarily safe and may exceed the safe operating voltage range for the module.

FIFO (First-In-First-Out) Buffer Size – A FIFO is a block of memory used to store a certain number of samples on the board so that data is not lost if the data cannot be transferred to computer memory fast enough. The FIFO is very important in high-speed DAQ products running with software such as Windows, which can have high interrupt latencies. The FIFO size is typically specified in number of samples so that you know how many sample points can be buffered. The amount of latency that the product can tolerate is determined by multiplying the ADC conversion time (1/sampling rate) by the size of the FIFO.

Data Transfers – The methods available to transfer digitized data from the DAQ board to computer memory. Options for data transfer are DMA, interrupt, and programmed I/O. For programmed I/O transfers, the CPU in the PC reads data from the DAQ board whenever the CPU receives a software code to acquire a single data point. Interrupt data transfers occur when the DAQ board sends an interrupt to the CPU, telling the CPU to read the acquired data from the DAQ board. DMA transfers use a DMA controller instead of the CPU to move acquired data from the board into computer memory. Even though high-speed data transfers can occur with interrupt and programmed I/O transfers, they require the use of the CPU to transfer data. DMA transfers are able to acquire data at high speeds and keep the CPU free for performing other tasks at the same time.

DMA Modes (only for boards with DMA transfer capability) – The methods of DMA transfer available to transfer digitized data from the DAQ board to computer memory. Options for DMA modes are single, demand, and block-mode transfers. In single-mode transfers, one data value is transferred for each DMA request asserted, which is the slowest method of transfer because the DMA controller must arbitrate for the system bus with each transfer. Block and demand transfer modes increase system throughput because the DMA controller performs several DMA transfers once the DMA controller has gained bus access. For block-mode transfers, the DMA controller performs the entire DMA sequence as specified by the transfer count register at the fastest possible rate in response to a single DMA request from the DAQ board. For demand-mode transfers, the DMA

controller performs DMA transfers at the fastest possible rate as long as the DAQ board asserts its DMA request. When the DAQ board unasserts this DMA request, transfers are held off. For more information on DMA modes, see Application Note 011, *DMA Fundamental on Various PC Platforms*.

Configuration Memory Size – The configuration memory contains the scan list information for analog input operations. Each entry in the configuration memory defines the behavior of each analog-to-digital conversion. The information includes, but is not limited to, channel number, polarity, gain, and dither.

Transfer Characteristics

Relative Accuracy – A measure in least significant bits (LSBs) of the nonlinear errors associated with a DAQ system. Relative accuracy is the worst-case deviation from the ideal DAQ board transfer function, a straight line. A relative accuracy test is run by linearly sweeping the input from minus full scale to plus full scale and comparing the average of the digitized values to the values of an endpoint-fit straight line, created from an endpoint fit of the data. Relative accuracy includes all nonlinearity and quantization errors but does not include offset and gain errors of the circuitry feeding the ADC. The relative accuracy is measured in least significant bits (LSBs). The lower the relative accuracy, the better the linearity of the product. Practically, a good DAQ product will have a relative accuracy of within ±1 LSB. The relative accuracy is a very important specification because it tells how accurately the continuous analog input range is converted to discrete digital values.

Nonlinearity – A measure in percent of FSR (full scale range) of the worst-case deviation from the ideal transfer function of a DAQ product, a straight line. This specification is included only for DAQ products such as signal conditioning products that do not have an ADC. Because a product with this specification will also be used with a DAQ product with an ADC, this nonlinearity specification must be added to the relative accuracy specification of the DAQ product with the ADC.

INL – INL is the acronym for integral nonlinearity, a measure in LSBs of the straightness of the transfer function of a DAQ board. Specifically, it indicates how far a plot of the DAQ board code transitions deviate from a straight line. The INL test is run by linearly sweeping the input from minus full scale to plus full scale and recording the locations of the transitions from one LSB to the next. The INL is the worst-case value found by subtracting the actual code transition locations from an endpoint-fit line of the transitions.

DNL – DNL is the acronym for differential nonlinearity, a measure in LSB of the worst-case deviation of code widths from their ideal value of 1 LSB. The DNL test is run by putting a triangle wave into one channel of the DAQ board, digitizing many cycles of the waveform, making a histogram of the data, and then normalizing the histogram. The greatest deviation from unity is the DNL. An ideal DAQ board has a DNL of 0 LSB, meaning all the codes have a width of exactly 1 LSB. Practically, a good DAQ board will have a DNL within ±0.5 LSB.

No Missing Codes – A missing code is a digital code that a DAQ board cannot produce, no matter voltage you input to it. A poorly performing DAQ board may have a code width equal to or very near zero, which causes a missing code. A missing code has a width of 0, causing the DNL to achieve the lower limit of –1 LSB. A DAQ board can be guaranteed to have no missing codes to the resolution of the board over a certain temperature range.

Offset Error – The additional voltage level, specified in volts, that can be introduced in the input circuitry. If you think of the amplifier transfer function as the equation $y = m\ (x + b_1) + b_2$, then b_1 is the pregain offset error and b_2 is the postgain offset error, where y is the output, x is the input, and m is the gain. A pregain offset error occurs before amplification and a post-gain offset error occurs after amplification. The pre-gain offset error will be amplified by the gain of the amplifier. The after-calibration specification shows the maximum offset that will occur when the board is calibrated properly. A before-calibration specification is also given so that you will know the worst-case error that can occur, even if the board is not calibrated. The before-calibration specification also includes the range of calibration of which the onboard circuitry is capable.

DC Offset Error – Same as offset error.

Gain Error – The degree to which the gain varies from the ideal, specified in percent of reading or ppm (parts per million) of reading. The after-calibration specification shows the maximum gain error that will occur when

the board is calibrated properly. A before-calibration specification is also given so that you will know the worst-case error that can occur, even if the board is not calibrated. The before-calibration specification also includes the range of calibration of which the onboard circuitry is capable. The specification also shows the error that will occur when the board is calibrated at a gain of 1 and used at a different gain.

DC Gain Error – The gain error on the DC component of the signal. This specification is not applicable when the device has AC input coupling.

Gain Adjustment Range – The range of gains for which the adjustment circuitry is capable of compensating.

Amplifier Characteristics

Input Impedance – The effective resistance and capacitance seen at the input to the amplifier. The impedance can vary differ when the board is powered on, powered off, and when isolated input limits are overloaded. In general, the higher the input impedance of the DAQ product, the less the product will disturb the signal being measured.

Input Bias Current – The current, specified in nA, produced by the analog input circuitry that flows through external components connected to the analog input channels. This current flowing through the resistance of the connected circuitry will add an unwanted voltage to the one that you are trying to measure. The lower the input bias current, the lower the additional unwanted voltage, and therefore the better the measurement.

Input Offset Current – The difference in the input bias currents of the two inputs of the instrumentation amplifier, usually specified in pA. If the source resistances connected to each of the input terminals are nearly the same and the input offset current is low, the resulting offset voltages tend to cancel. Thus, lower input offset currents improve measurements of balanced sources.

CMRR (Common-Mode Rejection Ratio) – CMRR describes the ability of a differential amplifier to reject interfering signals common to both inputs and amplify only the difference between the inputs. A differential-input instrumentation amplifier has both normal-mode (differential) gain and common-mode gain. The normal-mode gain is the amplification of the difference between the positive and negative inputs and ideally has such values as 1, 10, or 100. The common-mode gain refers to signals appearing at the output of the amplifier resulting from the same (that is, common) signals appearing at both of the inputs. Because the amplifier is expected to ignore common-mode signals, the common-mode gain is usually very low and is ideally zero. The CMRR is the ratio of the normal-mode gain to the common-mode gain and is usually expressed in dB. The higher the CMRR, the better the amplifier can extract differential signals in the presence of common-mode noise.

Output Range – A specification for external DAQ accessories such as signal conditioning that tells the voltage limits of the signal after it has been conditioned.

Output Impedance – The equivalent resistance at the output of external DAQ accessories such as signal conditioning accessories. The lower the output impedance, the better the signal accuracy.

Dynamic Characteristics

Bandwidth – The signal frequency range that is passed by the analog input circuitry. The bandwidth specification may have both a small signal bandwidth and a large signal bandwidth specification. The small signal bandwidth is the range of frequencies that is passed with attenuation less than –3 dB. Tests for small signal bandwidth are made with low voltage signals so that slew rate distortion is not a factor. The large signal bandwidth (also called the full power bandwidth) is the range of frequencies passed with THD less than a specified level, usually 1%. Tests for large signal bandwidth are usually made with full scale input signals. For most DAQ boards, the bandwidth is specified in Hz. For the dynamic signal acquisition boards that have digital antialiasing filters, the bandwidth is defined by the sampling rate.

AC Coupling Low-Frequency Cut-Off (–3 dB) – The –3 dB corner frequency of the high-pass filter that rejects the DC component of the input signal when the inputs are configured for AC coupling. This specification is important because it indicates which AC signals will be attenuated when AC coupling is used.

Settling-Time-to-Full-Scale Step – The amount of time required for a signal to reach a certain accuracy and stay within that range of accuracy. Settling time can be a major source of error for multichannel acquisition systems because the switching between channels can cause large voltage steps that the instrumentation amplifier may not be able to track quickly. National Instruments specifies how long it takes a worst-case step (from minus full scale to plus full scale) to settle to different accuracies. National Instruments Application Note 045, *Is Your Data Inaccurate Because of Instrumentation Amplifier Settling Time?*, gives an in-depth description of settling time.

Scan Interval – The minimum period between scans of multiple channels.

System Noise (including quantization error) – A measure of the amount of noise added by the analog circuit when the analog inputs are grounded at the I/O connector. On digitizers, this specification is given in LSBrms. For signal conditioning accessories, this specification is given in Vrms. The specification sometimes includes noise due to the quantization of the signal.

Dynamic Range – The ratio of the largest signal level a circuit can handle to the smallest signal level it can handle (usually taken to be the system noise level), expressed in dB. The dynamic range is equivalent to the maximum SNR.

Signal-to-THD Plus Noise – The ratio in dB of the rms test signal (a sine wave) to the rms level of residual harmonic distortion and noise. This specification must include the input level used to determine the specification and the bandwidth over which the specification is measured.

THD (Total Harmonic Distortion) – The ratio of the total harmonic distortion signal level to the test signal (sine wave) level. THD is usually expressed in dB, sometimes in percent.

Amplitude Flatness – A measure of how close to a constant the gain of a circuit remains over a range of frequencies. The specification is given in ± dB for a given frequency range.

Phase Linearity – A measure, in degrees, of the worst-case deviation of the phase-versus-frequency plot from a straight line.

Interchannel Phase – The difference in phase that may result when the same signal is connected to two or more channels. Unless otherwise stated, the interchannel phase is constant under constant operating conditions. Thus, you can test your system once to determine the interchannel phase and compensate for the error out additional tests.

IMD (Intermodulation Distortion) – IMD is the ratio, in dB, of the total signal level of harmonic sum and difference distortion products, to the overall test signal level. The test signal is two sine waves added together according to the following standards:

- SMPTE – A 60 Hz sine wave and a 7 kHz sine wave added in a 4:1 amplitude ratio
- DIN – A 250 Hz sine wave and an 8 kHz sine wave added in a 4:1 amplitude ratio
- CCIF – A 14 kHz sine wave and a 15 kHz sine wave added in a 1:1 amplitude ratio.

IMD reveals nonlinearities under AC input signal conditions as opposed to relative accuracy, which reveals nonlinearities under DC input signals conditions.

Overload Recovery Time – The time necessary for an amplifier saturated at full scale to recover from that saturation. In a multichannel acquisition, if the input of one channel saturates the amplifier and the scan period is shorter than the overload recovery time, the data read for the next channel in the scan may be erroneous.

Crosstalk – Any unwanted signal on one channel due to a signal on another channel. The crosstalk does not include any settling time error. Crosstalk is the ratio, in dB, of the level of the interference on the affected channel to the actual level of the interfering signal.

Filters

Type – Indicates what the purpose of the filter is. For example, simple single-pole RC filters are for noise rejection while more sophisticated hardware and digital FIR filters are suitable for antialiasing filters.

Cut-Off Frequency (–3 dB) – The frequency at which the filter attenuates the input 3 dB, or half of its original power. Stationary filters such as RC filters will express the cut-off frequency in Hz while digital antialiasing filters that move with the sampling rate will express the cut-off frequency in terms of the sample rate.

Programmable Values – The selectable values for the cut-off frequency on modules with programmable antialiasing filters. These switched capacitor filters are driven by a clock, either internal or external.

Maximum External Clock Frequency – The maximum external clock frequency usable to drive the switched capacitor programmable antialiasing filters.

Passband Ripple – Passband ripple indicates how much the analog signal will fluctuate due to the presence of the filters. The ripple is specified in dB for an input frequency range.

Stopband Attenuation – The minimum amount of attenuation that the filter provides in the stopband. The stopband is the range of frequencies where the filter attenuation is optimal.

Attenuation Rate – The slope with which the filter cuts off signals higher than the cut-off frequency. The attenuation rate will usually be specified in dB/octave. Filters on the dynamic signal acquisition boards are specified in dB per one-sixth octave because the filter attenuation is maximized in less than an octave.

NMR (Normal-Mode Rejection) – The amount of signal rejection at a certain frequency. Typically the frequency of the rejection is designed for electrical power frequencies such as 50 or 60 Hz.

Signal Delay – The amount of time required for the signal to be available for transfer to computer memory from the time the signal was present at the input to the DAQ board. This delay is specified on dynamic signal acquisition boards, which use delta-sigma modulating techniques, requiring a certain number of sample periods before the data is available at the output of the digital filter.

Sample-and-Hold (S/H) Characteristics

Acquisition Time – The time required for the sample-and-hold amplifiers to track to the correct voltage level of the input when coming out of hold mode. This specification is given for different tracking accuracies.

Hold-Mode Settling Time – The time necessary for the track-and-hold amplifiers to settle after the transition from track mode to hold mode.

Droop Rate – The rate, in V/s, at which a voltage drifts while being held by a sample-and-hold or track-and-hold circuit.

Interchannel Skew – The amount of delay that can occur between channels that are simultaneously sampled. The interchannel skew is usually specified in ns.

Intermodule Skew – Intermodule skew is specified on SCXI products to indicate the amount of delay that can occur between SCXI modules that are synchronized. The intermodule skew is usually specified in ns.

Aperture Delay Time – A measure of the interval between the time the digital sample signal occurs and the time when the actual analog sample is taken. A negative time value means that the propagation delay on the analog signal is greater than that of the digital sample signal.

Hold Step – The residual offset error of the track-and-hold amplifiers after the hold-mode settling time.

Aperture Jitter – The amount of variation in seconds of the aperture delay time. If a product has an external clock option, the specification will give the aperture jitter for both the internal and external clock.

Stability

Recommended Warm-Up Time – Because the electrical parameters of electronic components vary with temperature, stable and accurate electrical performance cannot be expected before the actual temperatures of the components are stable. The recommended warm-up time is the amount of time it takes for a room temperature unpowered product to stabilize at its higher operating temperature once it has been powered up.

Offset Temperature Coefficient – The sensitivity of the voltage offset of the product to changes in temperature. Usually, a pregain and a postgain offset temperature coefficient are specified. The coefficient is specified in µV/°C.

Gain Temperature Coefficient – The sensitivity of the gain of the product to changes in temperature. The coefficient is specified in ppm/°C.

Onboard Calibration Reference

Level – The voltage of the onboard reference of self-calibrating DAQ products. The level is usually specified as a voltage and a tolerance.

Temperature Coefficient – The sensitivity of the voltage of the onboard calibration reference to changes in temperature. The coefficient is specified in ppm/°C and sometimes in µV/°C.

Long-Term Stability – The amount of change in the onboard voltage reference with time. Long-term stability increases as parts age. Therefore, the stability is expressed in change per root time, usually in ppm/$\sqrt{1000}$ hour.

Analog Output

Output Characteristics

Number of Channels – The number of simultaneous analog signals that the product can generate.

Resolution – The number of bits that the digital-to-analog converter (DAC) uses to generate the analog signal. The higher the resolution, the higher the number of divisions the range is broken into, and therefore, the smaller the voltage step capable of being generated. Resolution is only one indication of DAQ product accuracy. You must consider at least the relative accuracy (linearity), offset errors, and gain errors to fully understand the accuracy of the DAQ product.

Common-Mode Isolation – The maximum allowable difference in voltage between the D/A converter channel and earth ground or another channel.

Max Update Rate – The fastest rate at which the analog output channels can convert digital data points to analog values. Some products can generate the analog output samples directly from a buffer of memory on the board and can therefore meet the max update rate under all conditions. Boards that have DMA data transfer capability can also meet the max update rate consistently because they have the DMA processor dedicated to transferring the data. Boards that require interrupt and programmed I/O transfers may not be able to consistently meet the max update rate because of the processor speed or other functions that the processor is trying to perform at the same time as transferring data to the analog outputs.

Type of DAC – Different applications require different types of digital-to-analog converters (DACs) for optimal performance. For example, an AC-class signal is best generated with a delta-sigma modulating DAC. Examples of common types of DACs are multiplying, double-buffered multiplying, and delta-sigma modulating.

FIFO (First-In-First-Out) Buffer Size – The FIFO is a block of memory used to store a certain number of samples on the board so that data can be continually generated, even when there are interrupt latencies preventing data transfers from PC memory. The FIFO size is specified in number of samples so that you know

how many sample points can be buffered. The amount of latency that the product can tolerate is determined by multiplying the DAC conversion time (1/update rate) by the size of the FIFO.

Data Transfers – Data transfers are the methods available to transfer digital data from computer memory to the DAQ board. Options are DMA, interrupt, and programmed I/O. For programmed I/O transfers, the CPU in the PC writes data to the DAQ board whenever the CPU receives a software code to generate a single analog value. Interrupt data transfers occur by the DAQ board causing an interrupt to the CPU, telling the CPU to write the digital data to the DAQ board. DMA transfers use a DMA controller instead of the CPU to move digital data from computer memory onto the DAQ board. Even though high-speed data transfers can occur with interrupt and programmed I/O transfers, they require the use of the CPU to transfer data. DMA transfers are able to move data at high speeds and keep the CPU free for performing other tasks at the same time.

DMA Modes (only for boards with DMA transfer capability) – This specification tells the methods of DMA transfer available to transfer data from computer memory to the analog output circuitry on the DAQ board. Options for DMA modes are single and demand transfers. In single-transfer mode, one data value is transferred for each DMA request assertion, which is the slowest method of transfer because the DMA controller must arbitrate for the system bus with each transfer. Demand-transfer mode increases system throughput because the DMA controller performs several DMA transfers once the DMA controller has gained bus access. For demand-mode transfers, the DMA controller performs DMA transfers at the fastest possible rate as long as the DAQ board asserts its DMA request. When the DAQ board unasserts this DMA request, transfers are held off. For more information on DMA modes, see Application Note 011, *DMA Fundamental on Various PC Platforms.*

Transfer Characteristics

Relative Accuracy (INL) – A measure in least significant bits (LSBs) of the nonlinear errors associated with a DAQ system. Relative accuracy is the worst-case deviation from the ideal analog output transfer function, a straight line. The lower the relative accuracy, the better the linearity of the product. Practically, a good analog output will have a relative accuracy within ±0.5 LSB. For analog output, the relative accuracy is the same as the INL. The relative accuracy may be dependent on the output range.

Absolute Accuracy – The furthest the voltage output will deviate from the calibrated reference as a percentage of full-scale range (FSR).

DNL (Differential Nonlinearity) – A measure in LSBs of the worst-case deviation of code widths from their ideal value of 1 LSB. An ideal DAQ board has a DNL of 0 LSB meaning all codes have a width of exactly 1 LSB. Practically, a good DAQ board will have a DNL within ±0.5 LSB.

Monotonicity – Monotonicity is the guarantee that the DAC will always give increasing voltages for increasing codes. Monotonicity can be guaranteed to a resolution (usually the resolution of the ADC) over a specified temperature range.

Offset Error – The additional voltage level, specified in volts, that can be introduced in the analog output circuitry. The after-calibration specification shows the maximum offset that will occur when the board is calibrated properly. A before-calibration specification is also given so that you will know the worst-case error that can occur, even if the board is not calibrated. The before-calibration specification also includes the range of calibration of which the onboard circuitry is capable.

Gain Error – The degree to which the gain varies from the ideal, specified in percent of reading or ppm of reading. The after-calibration specification shows the maximum gain error that will occur when the board is calibrated properly. A before-calibration specification is also given so that you will know the worst-case error that can occur, even if the board is not calibrated. The before-calibration specification also includes the range of calibration of which the onboard circuitry is capable. For self-calibrating DAQ products, the product will have an onboard reference. The gain error is often specified both for calibration relative to this internal reference and to an external calibration reference.

Voltage Output

Output Ranges – The voltage ranges that the board can generate. Output range is selected in hardware on some products and by software on others. The output range can be set by a voltage applied to the external reference input.

Output Coupling – The method by which the output signals are connected to the I/O connector. If the coupling is DC, both the AC and DC portions of signals are passed and generated. If the coupling is AC, then only the AC portions of signals are passed and any DC signals are rejected.

Output Impedance – The effective source resistance seen at the output of the analog output channel. The lower the output impedance, the less effect that circuitry connected to the analog outputs will affect the analog output signal.

Current Drive – The maximum amount of current that can be generated by an analog output channel.

Recommended Load Impedance – The recommended minimum resistance and maximum capacitance that the circuitry connected to the analog output should have.

Protection – The conditions that the analog output circuitry can be subject to without damaging the board. Common types of protection are short circuit to ground and open circuit.

Power-On State – The level of the analog output channels when the product is powered on.

External Reference Input – AC and DC signals can be connected to the external reference input to set the full scale levels of signals generated by the analog outputs.

Range – The range of voltage levels that can be connected to the external reference input without saturating.

Overvoltage Protection – This specification indicates the maximum voltage level that can be input to the external reference without damaging the board.

Input Impedance – The effective resistance and capacitance seen at the external reference input.

Bandwidth (–3 dB) – The range of frequencies that is passed with attenuation less than 3 dB.

Current Output

Range – The levels of current that can be controlled. Most current ranges will be 4 to 20 mA or 0 to 20 mA.

Type – Type indicates how the current output channel controls the current. Some outputs are current sinking channels, indicating that they require an external excitation source, while others can source the current without external sources.

Output Impedance – The effective resistance of the current output channel. The lower the output impedance, the less effect that circuitry connected to the analog outputs will affect the analog output signal.

Current Loop Supply – The internal current loop supply indicates the range of voltages that the internal loop supply can have when used as the loop supply for the current output channel. The external current loop supply is the range of voltages that the current output channels can use when the current output channel requires an external excitation source.

Excitation Voltage Range – The range of voltages that the current output channels can use when the current output channel requires an external excitation source.

Absolute Accuracy – The farthest deviation that the current output will be from the calibrated reference as a percentage of full-scale range (FSR).

Slew Rate – The maximum rate of current change per unit of time that the analog output channel is capable of.

Protection – Protection specifies the types of conditions that the analog output circuitry can be subject to without damaging the board. Common types of protection are short circuit to ground and open circuit.

Power-On State – The level of the analog output channels when the product is powered on.

Dynamic Characteristics

Settling Time – The amount of time required for a signal to be accurate to within the specified accuracy and to remain within that range of accuracy. The amount of time to settle depends on the voltage step the analog output channel is generating. Thus, the specification will indicate the voltage step, and the amount of time required to settle to within a specified accuracy.

Slew Rate – The maximum rate of voltage change of which the analog output channel is capable.

Noise – A measure of the amount of unwanted signal added by the analog output circuitry. The noise is measured in Vrms over a specified frequency range.

Dynamic Range – The ratio of the largest signal level that the analog output circuitry can generate to the smallest signal level it can generate (usually taken to be the noise level), expressed in dB. The dynamic range is equivalent to the maximum signal-to-noise ratio.

Signal-to-THD Plus Noise – The ratio in dB of the rms test signal (a sine wave) to the rms level of residual harmonic distortion and noise. This specification must tell which output level is used to determine the specification and over what bandwidth the specification is measured.

Amplitude Flatness – The measure of how close to a constant the gain of a circuit remains over a range of frequencies. The specification is given in ±dB for a given frequency range.

IMD (Intermodulation Distortion) – The ratio, in dB, of the total signal level of harmonic sum and difference distortion products, to the overall test signal level. The test signal is two sine waves added together according to the following standards:

- SMPTE – A 60 Hz sine wave and a 7 kHz sine wave added in a 4:1 amplitude ratio
- DIN – A 250 Hz sine wave and an 8 kHz sine wave added in a 4:1 amplitude ratio
- CCIF – A 14 kHz sine wave and a 15 kHz sine wave added in a 1:1 amplitude ratio

IMD reveals nonlinearities under AC input signal conditions as opposed to the relative accuracy which reveals nonlinearities under DC input signals conditions.

Crosstalk – Crosstalk, specified in dB, is any unwanted signal on one channel due to a signal on another channel.

Filter Characteristics

Type – The type of filter used on the analog output circuitry. Typical filter types are RC and digital interpolating FIR.

Cutoff Frequency (–3dB) – The frequency at which the filter attenuates 3 dB of the input. Stationary filters such as RC filters will express the frequency in Hz while anti-imaging filters that move with the update rate will express the cut-off frequency in terms of the update rate.

Signal Delay – The amount of time required for the signal to be present at the I/O connector from the time the analog output digital code was written to the DAQ board. This is specified on dynamic signal acquisition boards, which use delta-sigma modulating techniques, requiring a certain number of sample periods before the data is available at the output of the digital filter.

Stability

Offset Temperature Coefficient – The sensitivity of the voltage offset of the product to changes in temperature. The coefficient is specified in µV/°C.

Gain Temperature Coefficient – The sensitivity of the gain of the product to changes in temperature. The coefficient is specified in ppm/°C. The gain temperature coefficient is often specified both for calibration relative to this internal reference and to an external calibration reference.

Onboard Calibration Reference

Level – The voltage of the onboard reference of self-calibrating DAQ products. The level is usually specified as a voltage and a tolerance. Even though the tolerance on the calibration reference is large, the DAQ product can be accurately calibrated if the actual value of the calibration level is stored on the board in EEPROM. The calibration reference is selected for its stability over temperature and time, not for the absolute accuracy of its voltage level.

Temperature Coefficient – The sensitivity of the voltage of the onboard calibration reference to changes in temperature. The coefficient is specified in ppm/°C and sometimes in µV/°C.

Long-Term Stability – The amount of change in the onboard voltage reference with time. Long term stability increases as parts age. Therefore, the stability is expressed in change per root time, usually in ppm/$\sqrt{1000}$ hour.

Digital I/O

Number of Channels – The number of input or output digital signals that the DAQ product is capable of acquiring and generating. Some of the channels may be input or output, while others may always be inputs or always be outputs.

Compatibility – The compatibility indicates whether the digital I/O channels are TTL or CMOS compatible, or compatible with both.

Power-On State – The logic level to which the digital channels will be to when the product is first powered on. Possible power on states are logic low, logic high, and configured as input.

Digital Logic Levels – The minimum and maximum voltage levels that will be detected or generated as a low or high voltage. This specification will also indicate the current levels associated with the high and low voltages.

Input Low Voltage – The minimum and maximum voltages that the DAQ product will read as a low logic level (binary 0) for that digital channel.

Input High Voltage – The minimum and maximum voltages that the DAQ product will read as a high logic level (binary 1) for that digital channel. Voltage between the input low voltage max and the input high voltage min are indeterminate as to whether they will return a binary 0 or 1.

Input Low Current – The maximum current that the board can source at the specified voltage V_{in} when the digital channel is in the logic low state. The current is specified as a negative number to emphasize that current is being sourced by the DAQ product.

Input High Current – The maximum current that the board can sink at the specified voltage V_{in} when the digital channel is in the logic high state.

Output Low Voltage – The highest voltage the digital channel will generate at the output current I_{out} when the DAQ product is generating a logic low signal.

Output High Voltage – The lowest voltage the digital channel will generate at the output current I_{out} when the DAQ product is generating a logic high signal. The current is specified as a negative number to emphasize that current is being sourced by the DAQ product.

Output Low Current – The highest current that the digital output channel can sink while generating an output logic low signal V_{out}.

Output High Current – The highest current that the digital output channel can source while generating an output logic high signal V_{out}. The current is specified as a negative number to emphasize that current is being sourced by the DAQ product.

Darlington Drive Output Current – Darlington drive digital outputs are digital channels with higher current drive capability than typical digital channels. The Darlington drive output current specification indicates which ports have darlington drive capability. The specification also indicates the current the channel can source into a given resistance at a given voltage. The current is specified as a negative number to emphasize that current is being sourced by the DAQ product.

Input Impedance – The effective resistance and capacitance seen at the input to the digital input channels. In general, the higher the input impedance of the DAQ product, the less the product will disturb the signal being measured.

Common-Mode Isolation – The maximum allowable difference in voltage between a channel and earth ground or another channel.

Common-Mode Transient Rejection – The maximum allowable slew rate, expressed as V/µs, for the maximum working common mode voltage. In other words, if your working common mode voltage is changing more rapidly than this specified amount, the signal conditioning will not be able to reject the common mode voltage.

Transfer Rate – The rate at which the digital I/O board can read its digital inputs or change its digital outputs. The rate is highly dependent on the computer and software used, and what type of data transfer is used to move data to and from computer memory. The specification will often indicate the type of computer, software, and transfers used to achieve the specified rates. The rate will be specified in either bytes/*s* or words/*s* where a word can be specified as either 16 or 32 bits.

Propagation Delay – Specified for signal conditioning modules such as SCXI, is the time necessary, when the module is used in parallel mode, for a digital signal to propagate from the DIO board output to the output of the module, or from the input of the module to the DIO board input.

Handshaking – Handshaking indicates the available methods of handshaking data into and out of the digital I/O board. Some boards have dedicated handshaking lines while others require the sacrifice of one or more digital I/O ports to use the handshaking capabilities. With all handshaking, the data source and data sink devices control data transfer by using two wires. The “request” signal of the data source is connected to the “acknowledge” signal of the data sink, and the “acknowledge” signal of the data source is connected to the “request” signal of the data sink.

To begin a data transfer, the data source device drives data onto the data bus and asserts its “acknowledge” signal. It then waits for its “request” signal to be asserted. The data sink device waits for its “request” signal to be asserted and reads data off of the data bus when that condition is met. It then asserts its acknowledge signal after reading the data. When the data source device senses that its “request” signal has been asserted, it clears its “acknowledge” signal and the whole cycle repeats.

Data Transfers – This specification tells the methods available to transfer digitized data from the DAQ board to computer memory. Options for data transfer are DMA, interrupt, and programmed I/O. For programmed I/O transfers, the CPU in the PC reads data from the DAQ board whenever the CPU receives a software code to acquire a single data point. Interrupt data transfers occur by the DAQ board causing an interrupt to the CPU, telling the CPU to read the acquired data from the DAQ board. DMA transfers use a DMA controller instead of

the CPU to move acquired data from the board into computer memory. Even though high-speed data transfers can occur with interrupt and programmed I/O transfers, they require the use of the CPU to transfer data. DMA transfers are able to acquire data at high speeds and keep the CPU free for performing other tasks at the same time.

DMA Modes (only for boards with DMA transfer capability) – This specification tells the methods of DMA transfer available to transfer data between computer memory and the digital I/O channels on the DAQ board. Options for DMA modes are single and demand transfers. In single-transfer mode, one data value is transferred for each DMA request assertion, which is the slowest method of transfer mode because the DMA controller must arbitrate for the system bus with each transfer. Demand-transfer mode increases system throughput because the DMA controller performs several DMA transfers once the DMA controller has gained bus access. For demand-mode transfers, the DMA controller performs DMA transfers at the fastest possible rate as long as the DAQ board asserts its DMA request. When the DAQ board unasserts this DMA request, transfers are held off. For more information on DMA modes, see Application Note 011, *DMA Fundamental on Various PC Platforms*.

Digital Relays

Number of Relays – The number of channels the DAQ product can switch with relays.

Relay Type – This specification describes the capabilities of the relays used on the DAQ product. Options for relay type are single-pole double-throw (SPDT), latching, and nonlatching. SPDT relays, also called Form C, can switch one channel from a common (COM) terminal between a normally open (NO) and normally closed (NC) terminal. Latching relays maintain their latest state, even when powered down. Nonlatching relays return to their normally closed state at power down.

Maximum Input Voltage – The highest voltage that should be connected to any input terminal (channel to earth), or between any two terminals (channel to channel). The voltage level is usually specified in VAC and VDC.

Maximum Switching Voltage – The highest voltage that can be switched by the relays. A specification is usually given for both AC and DC signals.

Maximum Switching Capacity – The highest load, or power, that can be switched by a relay. This capacity is specified for both AC and DC loads. Because you can often switch larger voltages at lower currents, the specification will sometimes include two current/voltage combinations for AC and/or DC.

Minimum Switching Capacity – The amount of voltage and current required to ensure that the relay contacts will conduct electricity. At lower loads, the closed relay may not conduct and appear to be an electrical open circuit. This specification usually includes the current/voltage combinations for both AC and DC loads.

On Resistance – The resistance measured across closed relay contacts.

Output Capacitance – The capacitance across the solid-state relay outputs (i.e. between ‘CHAN’ and ‘COM’).

Leakage Current – The maximum current that can flow across the solid-state relay outputs (i.e. between ‘CHAN’ and ‘COM’) when the relay is in the off state.

Contact Material – The material, such as silver alloy, with which the relay contact is constructed.

Expected Life – The number of opening and closing operations the relays are capable of before failure. Mechanical life is the expected life with no electrical load applied to the relays. Electrical life is measured with the maximum (or specified) switching load applied.

Thermal Offset – The amount of thermoelectric voltage generated at the junction of two closed contacts. This voltage appears as an offset across the relay contacts.

Maximum Operating Speed – The highest switching speed, expressed as operations per minute or second, at which you can use the relays. An operation is defined as a relay set and reset cycle. The maximum operating speed is specified for two conditions—with maximum switching load applied, and with no load or low-level loads.

Relay Set Time – The amount of time from when the voltage is applied to the latching relay until the normally open (NO) contact closes.

Relay Reset Time – The amount of time from when the input to the latching relay is reset until the normally closed (NC) contact closes.

Relay Operate Time – The amount of time from when the voltage is applied to the nonlatching relay until the normally open (NO) contact closes.

Relay Release Time – The amount of time from when the input to the nonlatching relay is reset until the normally closed (NC) contact closes.

Timing I/O

Number of Channels – The maximum number of channels available for timing input and output. The product may have some channels that are general purpose counter/timers and other channels that are scalable frequency output only. It is common for a multifunction DAQ board to use some of the available counter/timer channels for more sophisticated DAQ operations such as interval scanning. All National Instruments E Series multifunction boards, however, do not require user-available counter timers, even when performing sophisticated DAQ operations.

Digital Logic Levels – The minimum and maximum voltage levels that will be detected or generated as a low or high voltage. This specification will also indicate the current levels associated with the high and low voltages.

Input Low Voltage – The minimum and maximum voltages that the DAQ product will read as a low logic level (binary 0) for that timing channel.

Input High Voltage – The minimum and maximum voltages that the DAQ product will read as a high logic level (binary 1) for that timing channel. Voltage between the input low voltage max and the input high voltage min are indeterminate as to whether they will return a binary 0 or 1.

Input Low Current – The maximum current that the board can source at the specified voltage V_{in} when the timing channel is in the logic low state. The current is specified as a negative number to emphasize that current is being sourced by the DAQ product.

Input High Current – The maximum current that the board can sink at the specified voltage V_{in} when the timing channel is in the logic high state.

Output Low Voltage – The highest voltage the timing channel will generate at the output current I_{out} when the DAQ product is generating a logic low signal.

Output High Voltage – The lowest voltage the digital channel will generate at the output current I_{out} when the DAQ product is generating a logic high signal. The current is specified as a negative number to emphasize that current is being sourced by the DAQ product.

Output Low Current – The highest current that the digital output channel can sink while generating an output logic low signal V_{out}.

Output High Current – The highest current that the digital output channel can source while generating an output logic high signal V_{out}. The current is specified as a negative number to emphasize that current is being sourced by the DAQ product.

Resolution – The number of bits available for the counter timers. The number of events that the counter can count is determined by:

$$\text{number of events} = 2^{\text{resolution}}$$

For example, a 16-bit counter can count 65,536 events. If the timers have both general purpose counter/timers and frequency scalers, then the specification will tell the resolution of both.

Compatibility – The specification indicates whether the digital I/O channels are TTL or CMOS compatible, or compatible with both.

Base Clock Available – DAQ boards with counter/timers have an onboard clock that can be used to set the frequency to clock the counter/timer. The base clock available specification tells the frequencies that this clock can be programmed to generate.

Base Clock Accuracy – The accuracy, specified in percent, of the frequency generated by the onboard clock.

Maximum Source Frequency – The highest frequency that can be counted by the counter/timer.

Minimum Source Pulse Duration – The length of time of the smallest pulse measurable by the counter/timer.

Minimum gate pulse duration – The length of time of the smallest pulse detectable at the gate input of the counter/timer.

Data Transfers – This specification tells the methods available to transfer digitized data from the DAQ board to computer memory. Options for data transfer are DMA, interrupt, and programmed I/O. For programmed I/O transfers, the CPU in the PC reads data from the DAQ board whenever the CPU receives a software code to acquire a single data point. Interrupt data transfers occur by the DAQ board causing an interrupt to the CPU, telling CPU to read the acquired data from the DAQ board. DMA transfers use a DMA controller instead of the CPU to move acquired data from the board into computer memory. Even though high-speed data transfers can occur with interrupt and programmed I/O transfers, they require the use of the CPU to transfer data. DMA transfers are able to acquire data at high speeds and keep the CPU free for performing other tasks at the same time.

DMA Modes (only for boards with DMA transfer capability) – This specification tells the methods of DMA transfer available to transfer data between computer memory and the digital I/O channels on the DAQ board. Options for DMA modes are single and demand transfers. In single-transfer mode, one data value is transferred for each DMA request assertion, which is the slowest method of transfer mode because the DMA controller must arbitrate for the system bus with each transfer. Demand-transfer mode increases system throughput because the DMA controller performs several DMA transfers once the DMA controller has gained bus access. For demand-mode transfers, the DMA controller performs DMA transfers at the fastest possible rate as long as the DAQ board asserts its DMA request. When the DAQ board unasserts this DMA request, transfers are held off. For more information on DMA modes, see Application Note 011, *DMA Fundamental on Various PC Platforms*.

Triggers

Analog Trigger

Source – The channels available that can be the source for the analog trigger.

Level – The range of levels that can be input as an analog trigger.

Slope – The description of whether the trigger should occur on an increasing voltage (positive slope) or a decreasing voltage.

Resolution – The number of bits used to determine the voltage level of the analog trigger. The higher the resolution, the higher the number of divisions the input range is broken into, and therefore, the smaller the detectable voltage change.

Hysteresis – The voltage level that defines the range that a signal must pass through after it has caused a trigger before the signal can cause a second trigger. Hysteresis prevents multiple triggers from occurring when there are small amounts of noise on the signal.

Bandwidth (–3dB) – The range of frequencies that can be input into the analog trigger.

External Input Impedance – The effective resistance and capacitance of the external analog trigger input.

Coupling – The method by which the input signals are connected to the trigger circuitry. If the coupling is DC, both the AC and DC levels will be passed to be used for a trigger. If the coupling is AC, then only the AC signals will be passed and the DC signals will be rejected.

Protection – The highest voltage levels that can be input to the trigger channel without damaging the board. Usually, a specification will be given for both the protection when the board is powered on and when the board is powered off. It is important to note that a low voltage signal that is riding on a high common mode voltage can damage the board if the combination of the two levels exceeds the levels for which the board is protected.

Digital Trigger

Compatibility – Indicates whether the digital trigger inputs are TTL or CMOS compatible, or compatible with both.

Response – Indicates if the trigger responds to an edge transition or a voltage level.

Pulse Width – The minimum pulse width that can activate the digital trigger.

Excitation

Output Characteristics

Channels – The number of independent excitation channels.

Bridge Types – The type of bridge sensor that can be used with the product (quarter, half, or full).

Bridge Completion – Description of the bridge completion circuitry (resistors) required when the product is measuring half or quarter bridge sensors. For example, bridge completion consisting of two resistors will comprise one half of a full bridge, with a half-bridge sensor comprising the other half.

Voltage Mode

Level – The voltage level of each excitation channel. This specification also includes the excitation channel accuracy (expressed as a percentage) and the maximum current that an excitation channel can drive. If the channel is configurable for different levels, all levels are listed.

Current Drive – The amount of current that the constant excitation voltage can source.

Drift – The rate at which the excitation voltage level will drift with temperature.

Current Mode

Level – The amount of current sourced by the excitation channel. This specification also includes the excitation channel accuracy (expressed as a percentage). If the channel is configurable for different levels, all levels are listed.

Max Load Resistance – The maximum resistance that an excitation current can drive with the specified current level. For example, an excitation channel with 10 kΩ load resistance limit can drive its specified current through up to ten 1 kΩ devices, or one hundred 100 Ω devices.

Drift – The rate at which the excitation current level will drift with temperature.

Cold-Junction Reference

Output – The range of voltages generated by the cold-junction temperature sensor. IC temperature sensors are linear and their output is expressed as mV/°C. A 10 mV/°C sensor, for example, will output 250 mV at 25°C. Thermistor outputs, however, are nonlinear. Therefore, thermistor output is specified as the voltage range over a defined temperature range (*x* volts at 50°C to *y* volts at 0°C).

Accuracy – The accuracy to which the temperature sensor measures the true cold-junction reference junction. This specification includes the inaccuracy of the sensor, any supporting components, inaccuracy of measuring the sensor output with an SCXI system and DAQ board, and inaccuracy caused by temperature gradients between the sensor and any of the screw terminals. The accuracy of the thermistor sensor on the SCXI-1328 varies over temperature; therefore, accuracy may be specified for particular operating temperature range.

Repeatability – This specification indicates how well the cold junction sensor can repeat its performance. This specification has nothing to do with how close the measurement is to the actual temperature (see Accuracy above); rather it describes the precision of the sensor in repeating the measurement. Therefore, offset and gain errors of the system are not included. Repeatability does include errors such as nonlinearity, noise, and the temperature gradient between the sensor and any of the screw terminals.

Digital Signal Processor

DSP Processor

DSP Processor – The type of DSP processor chip used on the plug-in board. DSP chips are designed as stand-alone processors that can run independent of the host CPU. DSP chip computation performance is optimized for math operations common to spectral analysis, such as the Fast Fourier Transform and convolution. In addition, DSP chips feature parallel multiply operations and can handle DMA transfers and interrupt requests.

Clock Speed – The rate at which the DSP chip is clocked.

Instruction Rate – A measure of how fast the DSP processor can execute instructions. The instruction rate is measured in millions of instructions per second (MIPS).

Floating-Point Rate – A measure of how fast the DSP processor can make floating point calculations. The floating-point rate is measured in millions of floating point operations per second (MFLOPS). The maximum MFLOPS equals the MIPS rating multiplied by the number of parallel floating-point operations that the DSP processor performs in one instruction cycle. DSP chips cannot sustain peak MFLOPS performance.

Memory

On-Chip – The amount of random access memory (RAM) located on the DSP chip. Typically the on-chip memory is accessed faster than the dual access or dual ported memory.

Dual-Ported – The amount of RAM that can be simultaneously accessed by more than one DMA controller or DSP processor.

Dual-Access – The amount of RAM that can only be accessed sequentially by controllers, CPU, or DSP chip.

DMA Controllers

Access – An indication of which memory the specified DMA controller can move data to and from.

Max Transfer Rate – The highest speed at which the DMA controller can move data from one point to another.

Number of Channels – The number of DMA channels available for data transfer by the specified DMA controller.

Interrupts

Types – The types of interrupts used by the DSP board.

Throughput Rates

1 Kword Transfer – Data transfer time required to transfer 1 Kword of data. The specification will indicate where the data is transferred from and to.

1 K FFT – DSP processor time needed to calculate a 1,024-point FFT.

RTSI

Trigger Lines – The number of trigger lines the board can connect to the RTSI bus.

Clock Skew – The delay that can occur on timing signals sent over the RTSI bus when used to synchronize events on two or more boards. This specification gives the time to get a signal to or from the RTSI connector on the board to the board function.

DMA Channels – For NuBus DAQ boards, this specification indicates the number of DMA channels available for the product to connect to the RTSI bus. The NB-DMA2800 board uses these timing signals to control the DMA data transfers.

Serial Links – The number of channels that a board can connect to the RTSI bus to send serial data between DAQ boards, without using the bus backplane. Usually, the type of data transfer is also specified. A full-duplex channel can send and receive data signals simultaneously. A half-duplex channel can either receive or send data but not simultaneously.

Serial Transfer Rate – The maximum rate at which data can be transferred serially over the RTSI bus serial channels.

Bus Interface – The type of interface the board has on its bus. The simplest boards are slaves, in which some other processor controls the operation of the bus and therefore the board. More sophisticated boards with processors often have master interfaces, so they can take control of the bus and control other boards that are plugged into the bus.

Power Requirement – Typically, the maximum amount of power that the board will require. This specification will tell the amount of power required from the different voltage signals available in the computer.

Physical

Dimensions – The size of the product. For plug-in boards, the dimensions will always be expressed in length and height

I/O Connector – Type of connector available on the product.

PCMCIA Card Type – Indicates the type of card for PCMCIA products.

Environment

Operating Temperature – The temperature range under which the components on the product can properly operate.

Storage Temperature – The temperature range under which the components on the product can be stored without damage.

Relative Humidity – The humidity range under which the components on the product can operate properly or be stored without damage.

Note: ***A "typical specification" provides good insight into how the product will perform because it represents how a vendor expects a product to perform under normal operating conditions. Typical specifications, however, are not binding specifications, and the product is not guaranteed to perform at the given specifications. Most companies give typical specifications because absolute maximum specifications are meaningless in many cases. For example, the absolute maximum power dissipation from a plug-in board could be calculated by determining the absolute maximum power dissipated by each component and adding them all together. This of course, would give a ridiculously high power usage specification that would never be reached by the board. Therefore, a more valuable specification is determined by using the board in normal operating conditions in a typical application and quoting the amount of power dissipated by the board in that application.***

With a "typical specification" the customer must rely on the honesty and integrity of the supplier. National Instruments gives very conservative typical specifications. When we hear that a customer is not achieving the typical specifications that we quote, we first attempt to verify the customers results and then redesign the product to meet the typical specifications, if necessary. If all else fails, we change the specifications to meet the performance of the product.

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